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12 December 2007

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Mr. Mark A. Haynes
HAYNES BEFFEL & WOLFELD LLP
P.O.Box 366, 637 Main Street
Half Moon Bay, Ca 94019
U.S.A

Japanese Patent Application No.: 2003-542509
Title: Method and Apparatus for Performing Computations on Data Using Data Steering
Your Ref: UNMI 1000-5 Our Ref: PJPF0022C1

HAYNES BEFFEL & WOLFELD LLP
DOCKETED: 12-13-07 BY: HK
ACTION: JP - OFFICE ACTION
DUE DATES: 12-30-07 INSTRUCT ASSOC.
1-30-08 DUE
DOCKET NO: UNMI 1000-5

Dear Mark:

The followings are an English translation of the first Official Action (Notification of reasons for rejection) to the above-referenced application mailed on 31 October 2007 and our comments.

Please provide us your instruction and proposal for claim amendments well before 30 January 2008. If we will not receive your instruction by 23 January 2008, we will submit a request for extension of the response time limit to the JPO. The three one-month extensions can be obtained with an official cost of JPY2,100/month.

[1] Notification of reasons for rejection:

Patent Application No.	2003-542509
Drafting Date	October 25, 2007
Examiner of JPO	Takashi Midorikawa 2950 5E00
Representative	Yoshifumi Masaki
Applied Provision	Section 29(2), Section 36, Section 37

ACKNOWLEDGED
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This application should be refused for the reasons mentioned

below. If the applicant has any arguments against the reason, such argument should be submitted within 3 months from the dispatch date of this notification.

Reasons

A. This application does not meet the requirements of Patent Law Section 37 due to the following reasons.

Note

The inventions described in the claims 23 to 28 and the claims 29 to 33 are not considered to have the relationship set forth in Patent Law Section 37(3) because they do not relate to a method of producing, a method of using, or a method of managing the data processing system according to claim 1 which comprises "a plurality of functional units, a plurality of routing units, responsive to routing control signals and coupled to the plurality of functional units, by which data is steered among the plurality of functional units, the routing control signals indicating a source functional unit and a destination functional unit for a data unit, and control word logic which supplies control words to the plurality of routing units, said control words including the routing control signals."

The examination of requirements for patent such as novelty or inventive step has not been carried out on the inventions according to claims other than the claims 1 to 22 because this application does not comply with the provision of Patent Law Section 37.

B. The descriptions of claims and detailed explanation of the inventions in this application do not meet the requirements of Patent Law Section 36(4) and (6)(ii) due to the following reasons.

Note

1. The claims 6 and 17 describe "the control word includes at least one of the write control signals and read control signals."
Since the claims 1 and 12 referenced by the dependent claims

6 and 17 describe "… supplies control words to the plurality of routing units" or "functional unit level control word logic which supplies signals the plurality of routing units, said control words including the routing control signals for the plurality of functional units", the "control words" can be recognized to be supplied to the routing units.

Thus, the technical meaning of supplying the write control signals and read control signals which are a part of the "control words" to the routing units cannot be understood.

2. The claims 7 and 18 describe "said control word includes an address for said memory."

However, as described above in paragraph 1, the "control words" of the claim 1 or 12 referenced by the dependent clams 7 and 18 would be supplied to the routing units. The technical meaning of supplying the address for said memory to the routing units cannot be understood.

3. The claim 12 describes "block level control word logic which supplies signals the plurality of processing blocks, said control word logic including the routing control signals for the processing blocks as the control words", but the technical meaning of supplying the routing control signals to the processing blocks cannot be understood. (The routing control signals should be supplied to the routing units.)

4. While the claims 16, 17 and 18 describe "the control word", the claim 12 referenced by these dependent claims describes both a block level "control word" and a unit level "control word." It is not clear which "control word" in the claim 12 is referenced by each of "the control word" in the claims 16, 17 and 18.

5. The claims 24 to 27 describe "the data processing method of claim 21", but the claim 21 describes "the data processing system", not "the data processing method." It is not clear what the description in the claims 24 to 27 indicates.

6. The claims 23 to 24, 29 and 33 describe "software control words" instead of "control words" described in the claims 1 and 12. The technical meaning of adding the term "software" cannot be understood and it is not clear what the term "software control words" means.

7. The claims 23 and 29 describe "providing (or supplying) a set of software control words", but do not describe an agent of the action. It is not clear whether the description means that a data processing engine transfers the software control words somewhere, that the software control words are inputted to a data processing device, that the software control words are transferred between circuits in the data processing device, or anything else. Its technical meaning cannot be understood.

8. If the description "providing (or supplying) a set of software control words" means compiling a software to generate control words, the description of the present application does not disclose specifically how to generate the control words from high-level programming languages such as Java, C, C++. The description does not also disclose what configuration the control words itself has. Therefore, the detail explanation of the inventions in this application is not described clearly and sufficiently to the extent that the person skilled in the art could put the inventions of the claims 23 to 33 into practice.

C. The inventions in the claims mentioned below of the subject application should not be granted a patent under Patent Law Section 29(2) since it could have easily been made by persons who have common knowledge in the technical field to which the inventions pertain, on the basis of the inventions described in the distributed publications mentioned below or made available to the public through electric telecommunication lines in Japan or foreign countries prior to the filing of the subject application.

Note (See the list of cited references etc., below.)
Claims 1-22

Cited References 1-4

Remarks:

The cited references 1 to 4 disclose a data processing system in which a plurality of function units are connected through a plurality of routing units such as switches and multiplexers. In addition, since the coupling state of the routing units can be modified, it is recognized that the data processing system comprises a means for supplying the routing control signals to the routing units.

It is a design choice which the person skilled in the art could implement in accordance with circumstances to include information for indicating a source functional unit and a destination functional unit in the routing control signals for specifying the coupling state.

In addition, it is only a design choice which the person skilled in the art could determine depending on processes performed in the data processing unit in accordance with circumstances what the functional units includes, whether a synchronous system is used or not, whether the functional units are grouped and constitute blocks or not.

If any reason(s) for rejection is found later, it will be notified.

Cited References

1. JP H09-294069 A
2. JP H11-219279 A
3. JP H10-111790 A
4. JP H06-274459 A

Record of the result of prior art search

- Technical field to be searched IPC G06F7/00-7/78
- Prior art documents JP 1991-033915 A

This record is not a component of the reasons for rejection.

[2] Our comments:

Regarding the reason A under Patent Law Section 37

We think the Examiner's assertion is reasonable. We think that claim 1 does not include any novel feature against the cited references, so that claims 1, 23 and 29 are recognized not to have any common unique features. We think it necessary to make the method claims 23 and 29 to depend from the apparatus claims 1 and 12, respectively.

Regarding the reason B under Patent Law Section 36(4) and (6-ii)

a) Regarding Notes 1 and 2:

We agree with the Examiner's opinion.

In Fig. 1, the routing control signals in the control word are applied only to the plurality of routing units. On the contrary, Fig. 2 clearly shows that other signals than the routing control signals in the control word, such as the write control signals and read control signals are applied to the functional units. We think that the control word is supplied not only the routing units but also the functional units. Thus, we think this should be clearly described in the dependent claims 6 and 17.

We think the same care will also be taken for the dependent claims 7 and 18.

b) Regarding Note 3:

We found an erroneous translation in claim 12, which made claim 12 unclear. This error can be corrected without your instruction.

c) Regarding Note 4:

We think the Examiner's assertion is reasonable. We think it necessary to clearly mention which "control word" in the claim 12 is referenced by each of "the control word" in the claims 16, 17 and 18. We think that "the control word" in the claims 16, 17 and 18 should be the unit level "control word", because "the control word" in the claims 16, 17 and 18 must be applied to a unit level of the function units according to their descriptions. Unfortunately, there is no detailed explanation about this matter in the description (paragraphs [0030] and [0031] of the PCT

application).

d) Regarding Note 5:

We think that claims 24 to 27 should depend from claim 23 instead of claim 21.

e) Regarding Notes 6-8:

We think the Examiner's assertion is reasonable and it very hard to overcome these rejections to claims 23-33 even if the rejection of reason A is resolved, since enough details about "software control words" are not explained in the description as the Examiner pointed out.

Regarding the reason C under Patent Law Section 29(2)

a) Brief explanations for the cited references 1-4:

R1) Reference 1 (JP H09-294069 A, published on 11 November 1997):

There is no corresponding US or EP application of R1.

R1 discloses a data processing system in which a plurality of function units are connected through a plurality of routing units such as switches and multiplexers, as Examiner noted.

Fig. 1 shows a basic circuit structure of programmable LSI. In Fig.1, function units PFU 1-15 (arithmetic units) include memories in which arithmetic function table is installed, and connected each other by crossbar switches (○), where ● shows a connection. In paragraph [0029], it is described that user can determine a type of the PFU's arithmetic function by controlling the crossbar switches.

Fig. 9 shows another embodiment of the programmable LSI. In Fig. 9, PFU block 100 is a LSI chip which includes 15 PFUs. PFU controller 200 and system controller 300 are prepared to be a set with PFU block 100. System controller 300 receives signals such as chip select signal CS, read signal RD, write signal WR and system addresses, and applies RD or WR signal to the PFU block 100 selected by CS signal. PFU controller 200 supplies signals based on system data input from outside such as func signal, PFU go signal, mux signal PFU sel signal, PFU done signal and clock enable signal. Fig. 10 shows a block diagram of the PFU block 100. In this case,

connections between PFUs in the PFU block 100 are fixed, but four outputs from PFUs 0, 8, 12, 14 can be output selectively by the mux signal. Thus, the function of the PFU block 100 is programmable. Multiplexer 101 functions as a kind of routing unit in the PFU block 100. Fig. 11 shows internal architecture of PFU, which includes FIFOs 110 for inputs, registers 111, selectors 112-113, multiplexing unit (MPU) 114, arithmetic logic unit (ALU) 115 and PFU instruction memory 116.

a2) Reference 2 (R2: JP H11-219279 A published on 10 August 1999):

US patent 6230175 is corresponding to parent application of R2.

R2 discloses a data processing system in which a plurality of function units are connected through a plurality of routing units such as multiplexers (selectors), as Examiner noted.

Fig. 6 shows reconfigurable digit serial multiplier and Fig. 9 shows reconfigurable digit serial arithmetic device. In Figs. 6 and 9, several digit multipliers with selector 41-46, which are arranged as a matrix, have digit multiplier #11-23 and selector S11-23, T11-23. In Fig. 9, the digit serial arithmetic device further includes digit serial adder-subtracters 111-113, each of which has digit serial adder-subtracters #31-33 and selector U31-33, V31-33.

Selectors S11-23, T11-23, U31-33, V31-33 work as routing units.

R3) Reference 3 (JP H10-111790 A published on 28 April 1998):

US patent 5805477 is corresponding to R3.

R3 discloses a data processing system in which a plurality of function units are connected through a plurality of routing units such as multiplexers (selectors), as Examiner noted.

Fig. 1 shows an arithmetic cell 100 of field programmable logic device, which includes steering logic circuits 101-107, flip-flop circuit 108, 16 bit look up table 109 as adder, switch transistor 110 and multiplexers 111-112. CF_1-CF_7, CF_ADDR and CF_FF are configuration signals. The steering logic circuits 101-107 are controlled by CF_1-CF_7 and the multiplexers 111-112 are controlled

by their respective control signals.

Fig. 2 shows 3x3 matrix of the arithmetic cell 100.

R4) Reference 4 (JP H06-274459 A published on 26 July 2002):

There is no corresponding US or EP application of R4.

R4 discloses a data processing system in which a plurality of function units are connected through a plurality of routing units such as crossbar switches (programmable switch array), as Examiner noted.

Fig. 1 shows LSI device comprising nonvolatile memory as micro-program memory. The device 120 includes master CPU 100, common memory 101, processors 102-103 with local memories, programmable switch arrays 105 and 109, I/O processors 106-108 and I/Os 111-119. Fig. 2 shows a block diagram of processors 102-103, which includes micro-program memory 201, decoder 210, register and arithmetic unit 211, local memory 212 and instruction register 213. The micro-program memory 201 includes writing and reading circuit 202, writing high-voltage circuit 203, memory array 204, address decoder 205, multiplexers 206 and 207, reading circuit 209 and micro-instruction register 209. Fig. 3 shows circuit structure of the programmable switch arrays 105 and 109, which includes n-channel type MOS transistor T11-T33 as switch element and nonvolatile memory cells M11-M33 connected to each gate electrode of the transistor T11-T33.

b) Differences between the instant invention and the cited references R1-R4:

As Examiner asserted, we think that the instant invention described in independent claim 1 is almost same as one disclosed by R1-R4. The limitations described in other dependent claims 2-11 are not so characteristic in comparison with R1. For example, R1 discloses the control word which includes the routing control signals (mux), write control signal (WR), read control signal (RD) and address signal for memory (system addresses) in Fig. 9.

As Examiner asserted such that it is only a design choice which the person skilled in the art could determine depending on processes performed in the data processing unit in accordance with

circumstances whether the functional units are grouped and constitute blocks or not, we think that the instant invention described in independent claim 12 does not include unique characteristic features in comparison with R1-R4. The limitations described in other dependent claims 13-22 are not so characteristic in comparison with R1.

Thus, we think the Examiner's assertion is quite reasonable at this moment.

Though we tried to find any characteristic points of the invention in the specification, we could not unfortunately reach to any good idea how to amend claims for overcoming the rejection of reason C.

We think that R1-R4 do not disclose about "software control words". However, we think it difficult to feature "software control words" in independent claims 1 and 12, since enough details about "software control words" are not explained in the description, as mentioned above.

Very truly yours,

Yoshifumi (Fred) Masaki
Masaki Patent Office

YM/mi

Enclosures:

1. Copies of each of the cited references R1-R4
2. Copies of the English translation of the abstract for the cited references R1-R4